CLAIMS

What is claimed is:

1. A semiconductor component comprising:

a leadframe having a surface;

an integrated passive component located above the surface of the leadframe;

a semiconductor chip electrically coupled to the integrated passive component and located above the surface of the leadframe; and

a mold compound disposed around the semiconductor chip, the integrated passive component, and the leadframe,

wherein:

a portion of the leadframe is exposed outside of the mold compound,

the integrated passive component comprises a passive device;

a direction perpendicular to the surface of the leadframe is a vertical direction; and

the semiconductor chip, the integrated passive component, and the leadframe are arranged vertically with respect to each other.

2. The semiconductor component of claim 1 wherein:

the passive device is not exposed at any surface of the integrated passive component.

3. The semiconductor component of claim 1 wherein:

the passive device is exposed at a surface of the integrated passive component.

4. The semiconductor component of claim 1 wherein:

the leadframe comprises a quad flat non-leaded leadframe.

5. The semiconductor component of claim 1 wherein:

the integrated passive component is located between the semiconductor chip and the leadframe.

6. The semiconductor component of claim 1 wherein:

the semiconductor chip is located between the integrated passive component and the leadframe.

7. The semiconductor component of claim 1 wherein:

the integrated passive component and the leadframe are electrically coupled together; and

the semiconductor chip and the leadframe are electrically coupled together.

8. A semiconductor component comprising:

a quad flat non-leaded leadframe having a surface;

an integrated passive component electrically coupled to the quad flat non-leaded leadframe;

a semiconductor chip electrically coupled to the integrated passive component; and

a mold compound disposed around the semiconductor chip, the integrated passive component, and the quad flat non-leaded leadframe,

wherein:

a portion of the quad flat non-leaded leadframe is exposed outside of the mold compound,

the integrated passive component comprises a passive device;

a direction perpendicular to the surface of the quad flat non-leaded leadframe is a vertical direction; and

the semiconductor chip, the integrated passive component, and the quad flat non-leaded leadframe are arranged vertically with respect to each other.

9. The semiconductor component of claim 8 wherein:

the integrated passive component comprises a multilayered structure having copper tracings forming a plurality of passive devices, including the passive device.

10. The semiconductor component of claim 8 wherein:

the passive device is not exposed at any surface of the integrated passive component.

11. The semiconductor component of claim 8 wherein:

the passive device is exposed at a surface of the integrated passive component.

12. The semiconductor component of claim 8 wherein:

the integrated passive component comprises a plurality of passive devices, including the passive device.

13. The semiconductor component of claim 12 wherein:

at least one of the plurality of passive devices is not exposed at any surface of the integrated passive component; and

at least one of the plurality of passive devices is exposed at a surface of the integrated passive component.

14. The semiconductor component of claim 8 wherein:

the integrated passive component is located between the semiconductor chip and the quad flat non-leaded leadframe.

15. The semiconductor component of claim 14 wherein:

the semiconductor chip is electrically coupled to the integrated passive component via a wire bond; and

the semiconductor chip is electrically coupled to the quad flat non-leaded leadframe.

16. The semiconductor component of claim 15 further comprising:

an adhesive layer located between the integrated passive component and the quad flat non-leaded leadframe,

wherein:

the adhesive layer secures the integrated passive component and the quad flat non-leaded leadframe to each other; and

the integrated passive component is electrically coupled to the quad flat non-leaded leadframe via the adhesive layer.

17. The semiconductor component of claim 14 further comprising:

an adhesive layer located between the integrated passive component and the quad flat non-leaded leadframe,

wherein:

the adhesive layer secures the integrated passive component and the quad flat non-leaded leadframe to each other;

the integrated passive component is electrically coupled to the quad flat non-leaded leadframe via the adhesive layer; and

the integrated passive component and the semiconductor chip are electrically coupled together using a flip chip interconnection.

18. The semiconductor component of claim 8 wherein:

the semiconductor chip is located between the integrated passive component and the quad flat non-leaded leadframe.

19. The semiconductor component of claim 8 wherein:

the semiconductor chip and the quad flat non-leaded leadframe are electrically coupled together using a flip chip interconnection; and

the integrated passive component is electrically coupled to the quad flat non-leaded leadframe via a first wire bond.

20. The semiconductor component of claim 19 wherein:

the integrated passive component is electrically coupled to the semiconductor chip via a second wire bond; and

the semiconductor chip is electrically coupled to the quad flat non-leaded leadframe via a third wire bond.

21. The semiconductor component of claim 8 wherein:

the integrated passive component comprises a material selected from the group consisting of silicon, gallium arsenide, silicon germanium, ceramic, glass, and organic polymer.

22. A method of manufacturing a semiconductor component, the method comprising:

providing a leadframe having a surface, the surface defining a horizontal direction and a line perpendicular to the surface defining a vertical direction;

attaching an integrated passive component to the leadframe, the integrated passive component comprising a passive device;

attaching a semiconductor chip to at least one of the integrated passive component and the leadframe such that:

the integrated passive component is located between the semiconductor chip and the leadframe; and

the semiconductor chip, the integrated passive component, and the leadframe have a vertical relationship with respect to each other; and

disposing a mold compound around the semiconductor chip, the integrated passive component, and the leadframe such that a portion of the leadframe is exposed outside of the mold compound.

23. The method of claim 22 wherein:

providing a leadframe comprises:

providing a quad flat non-leaded leadframe.

24. The method of claim 22 wherein:

attaching the semiconductor chip to at least one of the integrated passive component and the leadframe comprises:

wire bonding the semiconductor chip to at least one of the integrated passive component and the leadframe.

25. The method of claim 22 wherein:

attaching the semiconductor chip to at least one of the integrated passive component and the leadframe comprises:

electrically coupling the semiconductor chip to at least one of the integrated passive component and the leadframe using flip chip interconnects.

26. The method of claim 22 further comprising:

providing an adhesive layer between the integrated passive component and the leadframe; and

securing the integrated passive component to the leadframe using the adhesive layer.

27. A method of manufacturing a semiconductor component, the method comprising:

providing a leadframe having a surface, the surface defining a horizontal direction and a line perpendicular to the surface defining a vertical direction;

attaching a semiconductor chip to the leadframe;

attaching an integrated passive component to the semiconductor chip such that:

the semiconductor chip is located between the integrated passive component and the leadframe; and

the semiconductor chip, the integrated passive component, and the leadframe have a vertical relationship with respect to each other; and

disposing a mold compound around the semiconductor chip, the integrated passive component, and the leadframe such that a portion of the leadframe is exposed outside of the mold compound,

wherein:

the integrated passive component comprises a passive device.

28. The method of claim 27 wherein:

providing a leadframe comprises:

providing a quad flat non-leaded leadframe.

29. The method of claim 27 wherein:

attaching the semiconductor chip to the leadframe comprises:

electrically coupling the semiconductor chip to the leadframe using flip chip interconnects.

30. The method of claim 27 further comprising:

electrically coupling the integrated passive component to at least one of the semiconductor chip and the leadframe.

31. The method of claim 27 further comprising:

providing an adhesive layer between the integrated passive component and the semiconductor chip; and

securing the integrated passive component to the semiconductor chip using the adhesive layer.